PIC18F2XK20/4XK20

28/40/44-Pin Flash Microcontrollers with 10-Bit A/D and nanoWatt Technology

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 1.0 µA, typical
- Sleep mode current down to 0.1 µA, typical
- Timer1 Oscillator: 1.0 µA, 32 kHz, 1.8V, typical
- Watchdog Timer: 2.0 µA, 1.8V, typical
- Two-Speed Oscillator Start-up

Peripheral Highlights:

- High-current sink/source 25 mA/25 mA
- Three programmable external interrupts
- Four independent input-change interrupts
- 8 independent weak pull-ups
- Programmable slew rate
- Capture/Compare/PWM (CCP) module
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-Shutdown and Auto-Restart
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes with address mask
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN 2.0
  - RS-232 operation using internal oscillator block (no external crystal required)
  - Auto-Wake-up on Break
  - Auto-Baud Detect
- 10-bit, up to 14-channel Analog-to-Digital Converter module (ADC):
  - Auto-acquisition capability
  - Conversion available during Sleep
  - Internal 1.2V Fixed Voltage Reference (FVR) channel
  - Independent input multiplexing
- Dual analog comparators
  - Rail-to-rail operation
  - Independent input multiplexing
- Programmable On-Chip Voltage Reference (CV_{REF}) module (% of V_{DD})

Flexible Oscillator Structure:

- Four Crystal modes, up to 64 MHz
- 4X Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 64 MHz
- Internal oscillator block:
  - 8 user selectable frequencies, from 31 kHz to 16 MHz
  - Provides a complete range of clock speeds from 31 kHz to 64 MHz when used with PLL
  - User tunable to compensate for frequency drift
- Secondary oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if primary or secondary oscillator stops

Special Microcontroller Features:

- C compiler optimized architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- Self-programmable under software control
- Priority levels for interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-supply 3V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Operating voltage range: 1.8V to 3.6V
- Programmable 16-level High/Low-Voltage Detection (HLVD) module:
  - Supports interrupt on High/Low-Voltage Detection
- Programmable Brown-out Reset (BOR)
  - With software enable option

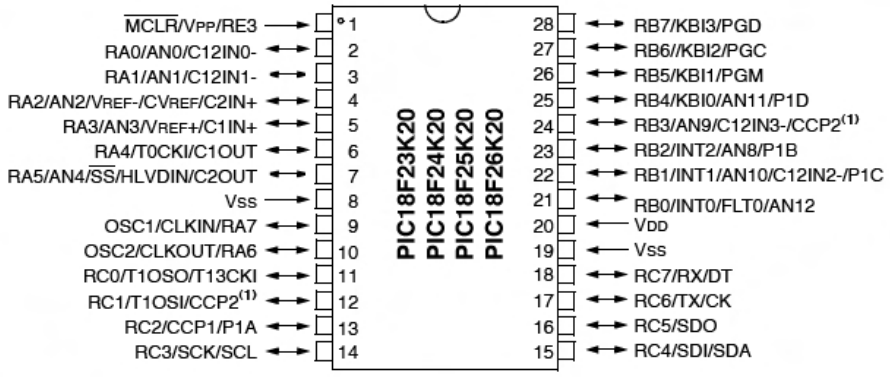
Device	Program Memory		Data Memory		I/O[1]	10-bit A/D (ch)[2]	CCP/ ECCP (PWM)	MSSP		EUSART	Comp.	Timers 8/16-bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I^2C™			
PIC18F23K20	8K	4096	512	256	25	11	1/1	Y	Y	1	2	1/3
PIC18F24K20	16K	8192	768	256	25	11	1/1	Y	Y	1	2	1/3
PIC18F25K20	32K	16384	1536	256	25	11	1/1	Y	Y	1	2	1/3
PIC18F26K20	64k	32768	3936	1024	25	11	1/1	Y	Y	1	2	1/3
PIC18F43K20	8K	4096	512	256	36	14	1/1	Y	Y	1	2	1/3
PIC18F44K20	16K	8192	768	256	36	14	1/1	Y	Y	1	2	1/3
PIC18F45K20	32K	16384	1536	256	36	14	1/1	Y	Y	1	2	1/3
PIC18F46K20	64k	32768	3936	1024	36	14	1/1	Y	Y	1	2	1/3

Note 1: One pin is input only.

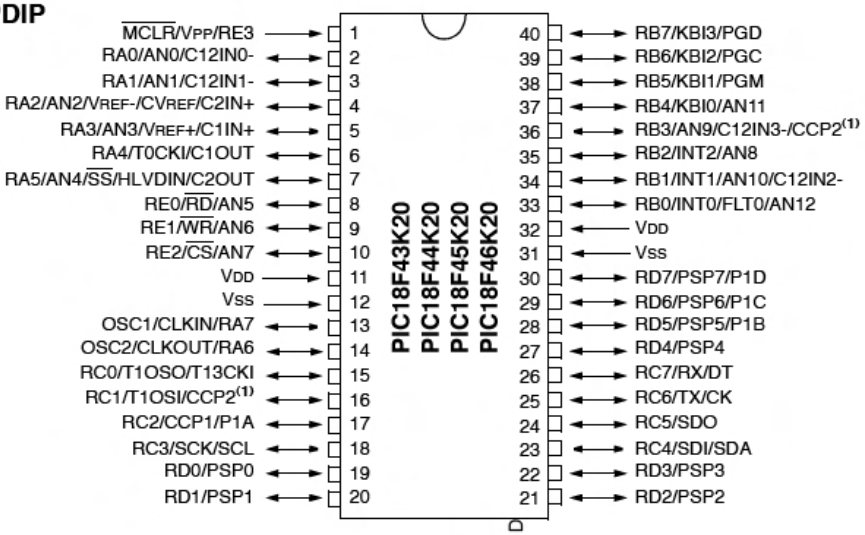
2: Channel count includes internal fixed voltage reference channel.

Pin Diagrams

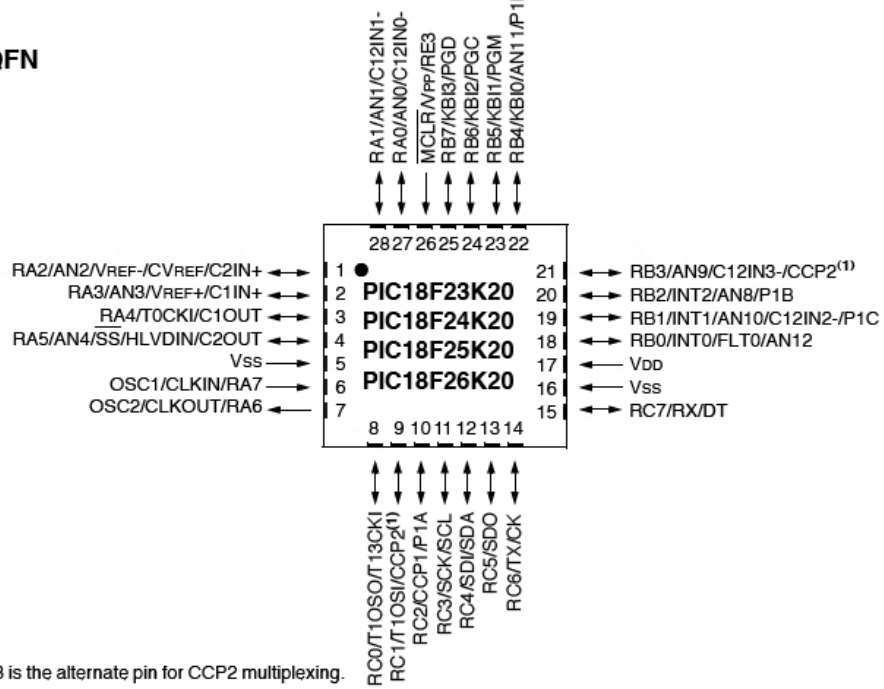
28-pin PDIP, SOIC, SSOP



40-pin PDIP



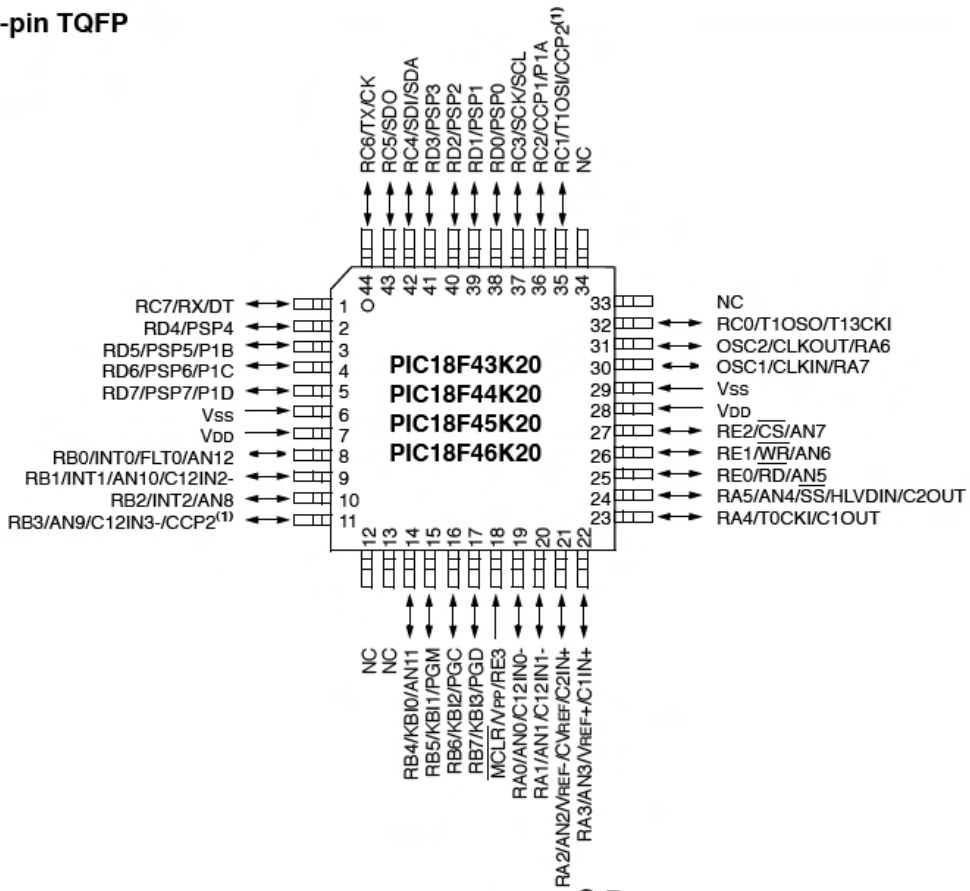
28-pin QFN



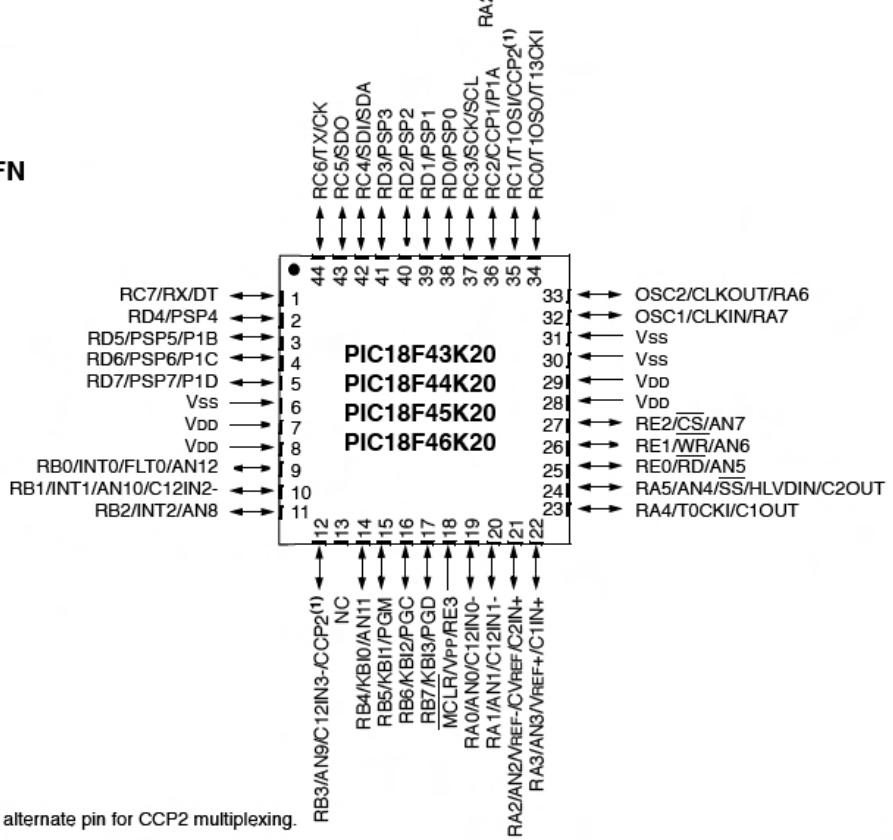
Note 1: RB3 is the alternate pin for CCP2 multiplexing.

Pin Diagrams (Cont.'d)

44-pin TQFP



44-pin QFN



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1: PIC18F4XK20 PIN SUMMARY

DIL Pin	TQFP Pin	QFN Pin	I/O	Analog	Comparator	Reference	ECCP	EUSART	MSSP	Timers	Slave	Interrupts	Pull-up	Basic
2	19	19	RA0	AN0	C12IN0-	—	—	—	—	—	—	—	—	—
3	20	20	RA1	AN1	C12IN1-	—	—	—	—	—	—	—	—	—
4	21	21	RA2	AN2	C2IN+	VREF-/ CVREF	—	—	—	—	—	—	—	—
5	22	22	RA3	AN3	C1IN+	VREF+	—	—	—	—	—	—	—	—
6	23	23	RA4		C1OUT	—	—	—	—	T0CKI	—	—	—	—
7	24	24	RA5	AN4	C2OUT	HLVDIN	—	—	$\overline{SS}$	—	—	—	—	—
14	31	33	RA6	—	—	—	—	—	—	—	—	—	—	OSC2/ CLKOUT
13	30	32	RA7	—	—	—	—	—	—	—	—	—	—	OSC1/CLKIN
33	8	9	RB0	AN12	—	—	FLT0	—	—	—	—	INT0	Yes	—
34	9	10	RB1	AN10	C12IN2-	—	—	—	—	—	—	INT1	Yes	—
35	10	11	RB2	AN8	—	—	—	—	—	—	—	INT2	Yes	—
36	11	12	RB3	AN9	C12IN3-	—	CCP2(1)	—	—	—	—	—	Yes	—
37	14	14	RB4	AN11	—	—	—	—	—	—	—	KBI0	Yes	—
38	15	15	RB5	—	—	—	—	—	—	—	—	KBI1	Yes	PGM
39	16	16	RB6	—	—	—	—	—	—	—	—	KBI2	Yes	PGC
40	17	17	RB7	—	—	—	—	—	—	—	—	KBI3	Yes	PGD
15	32	34	RC0	—	—	—	—	—	—	T1OSO/ T13CKI	—	—	—	—
16	35	35	RC1	—	—	—	CCP2(2)	—	—	T1OSI	—	—	—	—
17	36	36	RC2	—	—	—	CCP1/ P1A	—	—	—	—	—	—	—
18	37	37	RC3	—	—	—	—	—	SCK/ SCL	—	—	—	—	—
23	42	42	RC4	—	—	—	—	—	SDI/ SDA	—	—	—	—	—
24	43	43	RC5	—	—	—	—	—	SDO	—	—	—	—	—
25	44	44	RC6	—	—	—	—	TX/CK	—	—	—	—	—	—
26	1	1	RC7	—	—	—	—	RX/DT	—	—	—	—	—	—
19	38	38	RD0	—	—	—	—	—	—	—	PSP0	—	—	—
20	39	39	RD1	—	—	—	—	—	—	—	PSP1	—	—	—
21	40	40	RD2	—	—	—	—	—	—	—	PSP2	—	—	—
22	41	41	RD3	—	—	—	—	—	—	—	PSP3	—	—	—
27	2	2	RD4	—	—	—	—	—	—	—	PSP4	—	—	—
28	3	3	RD5	—	—	—	P1B	—	—	—	PSP5	—	—	—
29	4	4	RD6	—	—	—	P1C	—	—	—	PSP6	—	—	—
30	5	5	RD7	—	—	—	P1D	—	—	—	PSP7	—	—	—
8	25	25	RE0	AN5	—	—	—	—	—	—	$\overline{RD}$	—	—	—
9	26	26	RE1	AN6	—	—	—	—	—	—	$\overline{WR}$	—	—	—
10	27	27	RE2	AN7	—	—	—	—	—	—	$\overline{CS}$	—	—	—
1	18	18	RE3(3)	—	—	—	—	—	—	—	—	—	—	$\overline{MCLR}$/VPP
11	7	7	—	—	—	—	—	—	—	—	—	—	—	VDD
32	28	28	—	—	—	—	—	—	—	—	—	—	—	VDD
12	6	6	—	—	—	—	—	—	—	—	—	—	—	VSS
31	29	30	—	—	—	—	—	—	—	—	—	—	—	VSS
–	NC	8	—	—	—	—	—	—	—	—	—	—	—	VDD
–	NC	29	—	—	—	—	—	—	—	—	—	—	—	VDD
—	NC	31	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: CCP2 multiplexed with RB3 when CONFIG3H<0> = 0
2: CCP2 multiplexed with RC1 when CONFIG3H<0> = 1
3: Input only.

TABLE 2: PIC18F2XK20 PIN SUMMARY

Pin DIL	Pin QUAD	I/O	Analog	Comparator	Reference	ECCP	EUSART	MSSP	Timers	Slave	Interrupts	Pull-up	Basic
2	27	RA0	AN0	C12IN0-									
3	28	RA1	AN1	C12IN1-									
4	1	RA2	AN2	C2IN+	VREF-/ CVREF								
5	2	RA3	AN3	C1IN+	VREF+								
6	3	RA4		C1OUT					T0CKI				
7	4	RA5	AN4	C2OUT	HLVDIN			$\overline{SS}$					
10	7	RA6											OSC2/ CLKOUT
9	6	RA7											OSC1/ CLKIN
21	18	RB0	AN12			FLT0					INT0	Yes	
22	19	RB1	AN10	C12IN2-		P1C					INT1	Yes	
23	20	RB2	AN8			P1B					INT2	Yes	
24	21	RB3	AN9	C12IN3-		CCP2(1)						Yes	
25	22	RB4	AN11			P1D					KBI0	Yes	
26	23	RB5									KBI1	Yes	PGM
27	24	RB6									KBI2	Yes	PGC
28	25	RB7									KBI3	Yes	PGD
11	8	RC0							T1OSO/ T13CKI				
12	9	RC1				CCP2(2)			T1OSI				
13	10	RC2				CCP1/ P1A							
14	11	RC3						SCK/ SCL					
15	12	RC4						SDI/ SDA					
16	13	RC5						SDO					
17	14	RC6					TX/CK						
18	15	RC7					RX/DT						
1	26	RE3(3)											$\overline{MCLR}$/ VPP
8	5												VSS
19	16												VSS
20	17												VDD

Note 1: CCP2 multiplexed with RB3 when CONFIG3H<0> = 0
2: CCP2 multiplexed with RC1 when CONFIG3H<0> = 1
3: Input only

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1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F23K20
- PIC18F24K20
- PIC18F25K20
- PIC18F26K20
- PIC18F43K20
- PIC18F44K20
- PIC18F45K20
- PIC18F46K20

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Flash program memory. On top of these features, the PIC18F2XK20/4XK20 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2XK20/4XK20 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 26.0 "Electrical Characteristics"** for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2XK20/4XK20 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O)
- Two External RC Oscillator modes with the same pin options as the External Clock modes
- An internal oscillator block which contains a 16 MHz HFINTOSC oscillator and a 31 kHz LFINTOSC oscillator which together provide 8 user selectable clock frequencies, from 31 kHz to 16 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the high-speed crystal and internal oscillator modes, which allows clock speeds of up to 64 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 64 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

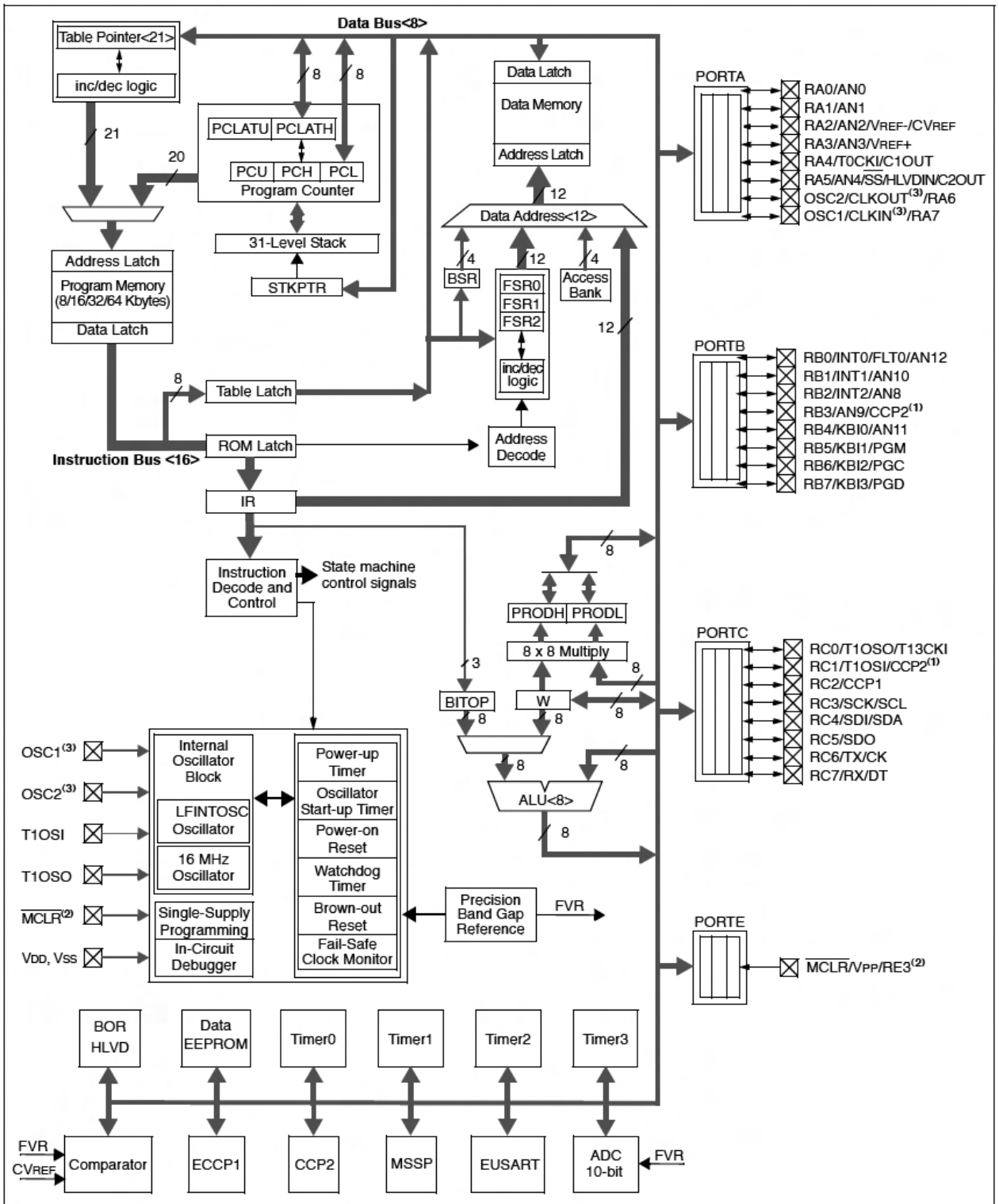
- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F23K20	PIC18F24K20	PIC18F25K20	PIC18F26K20	PIC18F43K20	PIC18F44K20	PIC18F45K20	PIC18F46K20
Operating Frequency	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
Program Memory (Instructions)	4096	8192	16384	32768	4096	8192	16384	32768
Data Memory (Bytes)	512	768	1536	3936	512	768	1536	3936
Data EEPROM Memory (Bytes)	256	256	256	1024	256	256	256	1024
Interrupt Sources	19	19	19	19	20	20	20	20
I/O Ports	A, B, C, (E)(1)	A, B, C, (E)(1)	A, B, C, (E)(1)	A, B, C, (E)(1)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
Timers	4	4	4	4	4	4	4	4
Capture/Compare/PWM Modules	1	1	1	1	1	1	1	1
Enhanced Capture/Compare/PWM Modules	1	1	1	1	1	1	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	No	No	No	No	Yes	Yes	Yes	Yes
10-bit Analog-to-Digital Module	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

Note 1: PORTE contains the single RE3 read-only bit. The LATE and TRISE registers are not implemented.

FIGURE 1-1: PIC18F2XK20 (28-PIN) BLOCK DIAGRAM

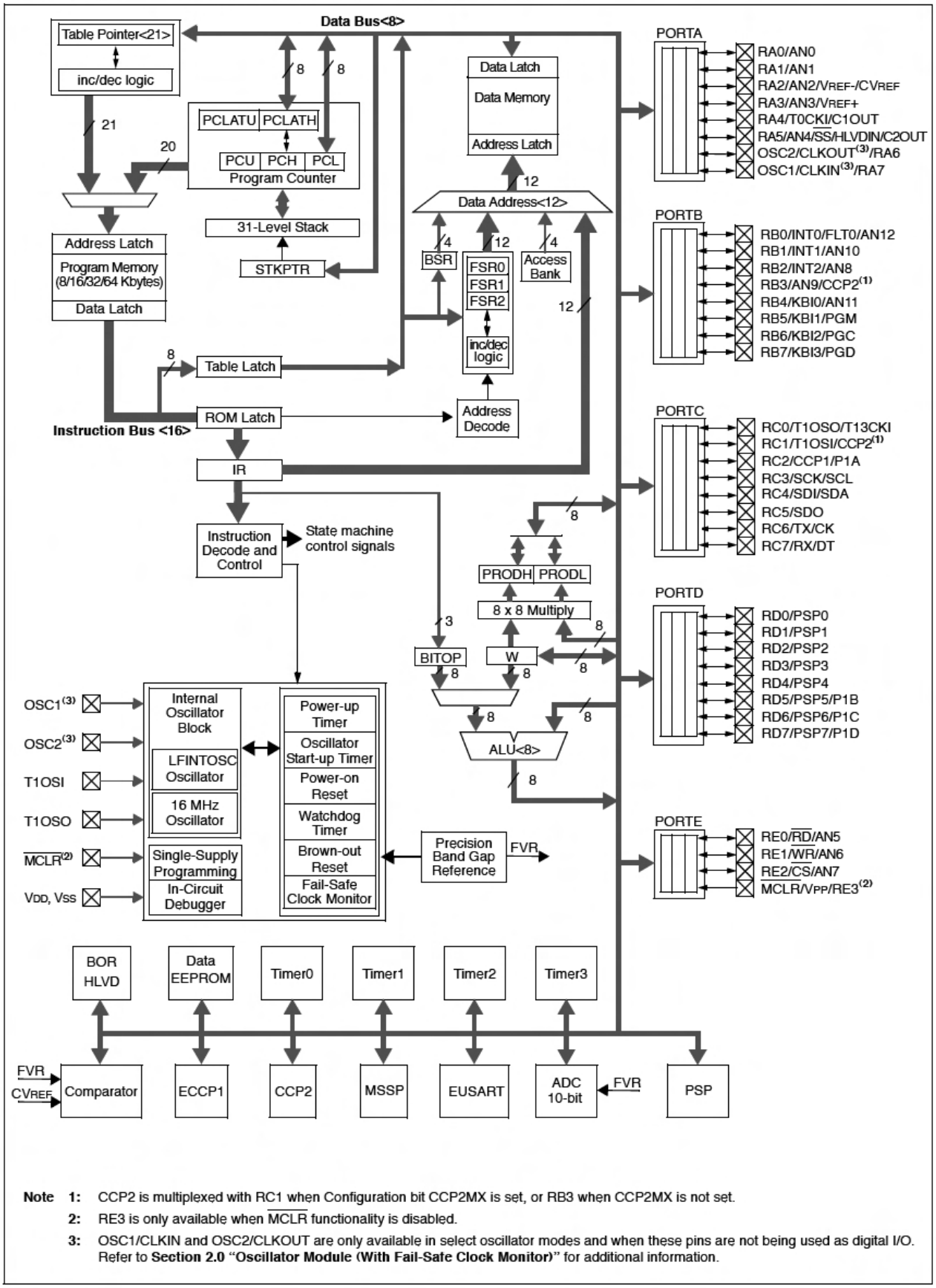


Note 1: CCP2 is multiplexed with RC1 when Configuration bit CCP2MX is set, or RB3 when CCP2MX is not set.

2: RE3 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

3: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional information.

FIGURE 1-2: PIC18F4XK20 (40/44-PIN) BLOCK DIAGRAM



Note 1: CCP2 is multiplexed with RC1 when Configuration bit CCP2MX is set, or RB3 when CCP2MX is not set.

2: RE3 is only available when MCLR functionality is disabled.

3: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional information.

TABLE 1-2: PIC18F2XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
$\overline{MCLR}$/VPP/RE3	1	26			Master Clear (input) or programming voltage (input)
$\overline{MCLR}$			I	ST	Active-low Master Clear (device Reset) input
VPP			P		Programming voltage input
RE3			I	ST	Digital input
OSC1/CLKIN/RA7	9	6			Oscillator crystal or external clock input
OSC1			I	ST	Oscillator crystal input or external clock source input ST buffer when configured in RC mode; CMOS otherwise
CLKIN			I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKIN, OSC2/CLKOUT pins)
RA7			I/O	TTL	General purpose I/O pin
OSC2/CLKOUT/RA6	10	7			Oscillator crystal or clock output
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode
CLKOUT			O	—	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
RA6			I/O	TTL	General purpose I/O pin

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-2: PIC18F2XK20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP, SOIC	QFN			
					PORTA is a bidirectional I/O port.
RA0/AN0/C12IN0-	2	27			
RA0			I/O	TTL	Digital I/O
AN0			I	Analog	Analog input 0, ADC channel 0
C12IN0-			I	Analog	Comparators C1 and C2 inverting input
RA1/AN1/C12IN1-	3	28			
RA1			I/O	TTL	Digital I/O
AN1			I	Analog	ADC input 1, ADC channel 1
C12IN1-			I	Analog	Comparators C1 and C2 inverting input
RA2/AN2/VREF-/CVREF/ C2IN+	4	1			
RA2			I/O	TTL	Digital I/O
AN2			I	Analog	Analog input 2, ADC channel 2
VREF-			I	Analog	A/D reference voltage (low) input
CVREF			O	Analog	Comparator reference voltage output
C2IN+			I	Analog	Comparator C2 non-inverting input
RA3/AN3/VREF+/C1IN+	5	2			
RA3			I/O	TTL	Digital I/O
AN3			I	Analog	Analog input 3, ADC channel 3
VREF+			I	Analog	A/D reference voltage (high) input
C1IN+			I	Analog	Comparator C1 non-inverting input
RA4/T0CKI/C1OUT	6	3			
RA4			I/O	ST	Digital I/O
T0CKI			I	ST	Timer0 external clock input
C1OUT			O	CMOS	Comparator C1 output
RA5/AN4/$\overline{SS}$/HLVDIN/ C2OUT	7	4			
RA5			I/O	TTL	Digital I/O
AN4			I	Analog	Analog input 4, ADC channel 4
$\overline{SS}$			I	TTL	SPI slave select input
HLVDIN			I	Analog	High/Low-Voltage Detect input
C2OUT			O	CMOS	Comparator C2 output
RA6					See the OSC2/CLKOUT/RA6 pin
RA7					See the OSC1/CLKIN/RA7 pin

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.